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week, built-in self-test (BIST) and design-for-test (DFT) dominated discussions of how to fight the astronomical costs of automated test equipment.

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Model environment backs design process

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December 14, 1999 - **Electronic Engineering Times**

Richard Drohan, Embedded Systems Program Manager, The MathWorks Inc., Natick, Mass.

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September 28, 1999 - **Electronic Engineering Times**

John Ousterhout, President, Scriptics Corp., Mountain View, Calif.

Increases in processor speed and memory sizes are making it possible to incorporate scripting in embedded systems themselves.

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Memory-test war flares at International Test Conference

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October 21, 1998 - **Electronic Engineering Times**

Stan Runyon

Evidence of a full-fledged memory-test war emerged this week at the International Test Conference as automatic test equipment (ATE) vendors rushed to satisfy the lofty speed and accuracy needs of such emerging DRAM architectures as Rambus.

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Embedded SRAM test and repair moves on-chip

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July 11, 2001 - **Electronic Engineering Times**

Anthony Cataldo, Anthony Cataldo

With the rollout of its Star Memory System, an on-chip test and repair mechanism for embedded SRAM, memory compiler specialist Virage Logic Corp. is making good on its promise to provide a way for chip companies to shuck their back-end memory testers.

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EEMBC slims down chip tests

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Mark Hachman

Sales defeated engineering on Wednesday (Jan. 3), as the EDN Embedded Microprocessor Benchmark Consortium (EEMBC) testing organization agreed to provide a simpler metric for evaluating the performance of embedded microprocessors.

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Standard test language to verify SoC

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Rohit Kapur, Principal Engineer, R.Chandramouli, Product Line Manager, Test Automation Group, Synopsys Inc., Mountain View, Calif.

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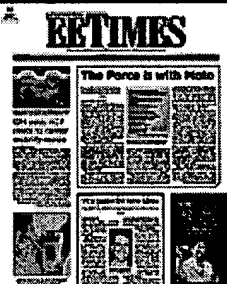
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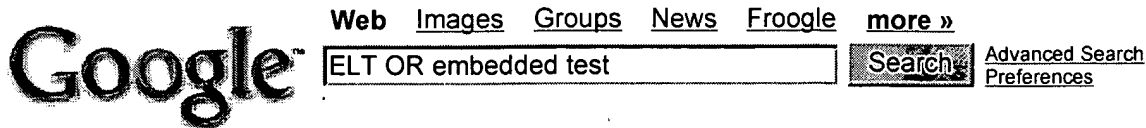
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2 Test data compression and compaction for embedded test of nanometer technology designs*Rajski, J.; Tyszer, J.;*

Computer Design, 2003. Proceedings. 21st International Conference on , 13-15 Oct. 2003

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3 End-to-end testing for boards and systems using boundary scan*Barr, R.W.; Chen-Huan Chiang; Wallace, E.L.;*

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5 Testing systems on a chip

Chandramouli, R.; Pateras, S.;

Spectrum, IEEE , Volume: 33 , Issue: 11 , Nov. 1996

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6 A pragmatic, systematic and flexible synthesis for testability methodology

Alves, V.C.; Antunes, A.R.; Marzouki, M.;

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